WHAT IS CLAIMED IS:

1. An integrated circuit comprising:

a plurality of logic cells; and

a rearrangeable programmable network interconnecting said logic cells, said programmable interconnection network having:

a plurality of programmable switches, each programmable switch having a plurality of input terminals and a number of output terminals, signals on any input terminal passed to any output terminal responsive to a programming of said switch,

said plurality of programmable switches arranged in a Benes network so as to form a rearrangeable network.

2. The integrated circuit of claim 1 wherein each of said programmable switches has two input terminals.

3. The integrated circuit of claim 1 wherein said integrated circuit comprises an FPGA.

4. The integrated circuit of claim 1 wherein each programmable switch has a plurality of latches responsive to clock signals for passing signals through said programmable interconnection network in a pipelined fashion to avoid uncertainties in signal routing delays through said programmable interconnection network.

5. The integrated circuit of claim 1 wherein predetermined ones of programmable switches each have a plurality of latches responsive to clock signals for passing signals through said programmable interconnection network in a pipelined fashion to avoid uncertainties in signal routing delays through said programmable interconnection network.